TP 16.5 Sense Amplifier-Based Flip-Flop

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Timing elements, latches and flip-flops, are critical to performance of digital systems, due to tighter timing constraints and low power requirements [1,5]. Short setup and hold times are essential, but often overlooked.

Recently reported flip-flop structures achieved small delay between the latest point of data arrival and output transition. Typical representatives of these structures are sense amplifier-based flip-flop (SAFF), hybrid latch - flip-flop (HLFF) and semi-dynamic flip-flop (SDFF) [4, 8, 9]. Hybrid flip-flops outperform reported sense-amplifier-based designs, because the later are limited by the output latch implementation.

SAFF consists of the sense amplifier in the first stage and the R-S latch in the second stage, Figure 16.5.1 [4].

The first stage of this flip-flop is the sense amplifier [2,3]. It senses the true and complementary differential inputs. The sense amplifier stage produces monotonous transitions from high to low logic level on one of the outputs, following the leading clock edge. The S-R latch captures each transition and holds the state until the next leading clock edge arrives. Therefore, the whole structure acts as a flip-flop.

The S-R latch operates as follows. Input $\overline{S}$ is a set input and $\overline{R}$ is a reset input. The low level at both $\overline{S}$ and $\overline{R}$ node is not permitted, guaranteed by the sense-amplifier stage. The low level at $\overline{S}$ sets the Q output to high, which in turn forces $\overline{Q}$ to low. Conversely, the low-level at $\overline{R}$ sets the $\overline{Q}$ high, which in turn forces Q to low. Therefore, one of the output signals is always delayed with respect to the other. The rising edge always occurs first, after one gate delay, and the falling edge occurs after two gate delays. This limits the performance of the SAFF.

The SAFF, shown in Figure 16.5.2, has the advantages of earlier published SAFFs. It allows integration of the logic into the flip-flop, as well as reduced clock swing operation [6]. The single-ended input version with multiplexed data scan and asynchronous reset is possible as shown in Figure 16.5.3.

The output stage takes advantage of two possible logic representations for the output Q: $Q=S+\overline{R}Q'$ and $Q=\overline{R}\cdot(S+Q')$, to produce four topologically equivalent pull-up and pull-down transistor networks, as shown in Figure 16.5.2. Given that the output stage is symmetric with respect to pull-up and pull-down circuits for Q and $\overline{Q}$, both pull-ups and pull-downs can be implemented using the same circuit topology, thus making the output stage symmetrical. The circuit topology has only one transistor in each branch active in changing state, allowing smaller keeper transistors, as illustrated in Figure 16.5.2.

The true and complementary trees are symmetrical, resulting in equal delays of both outputs, Figure 16.5.4. Since the keeper transistors, M_{P7}-M_{P10} and M_{N9}-M_{N12}, are minimized, they quickly switch off during the transition, which allows outer driver transistors, M_{P5}, M_{P6}, M_{N7} and M_{N8}, to drive the load, and change the state of the latch. This allows for a straightforward output transistor size optimization.

The SAFF is in 0.18μm effective channel length CMOS technology. Transistor sizing is optimized for both high speed and compact standard-cell layout.

Simulated flip-flop waveforms, shown in Figure 16.5.4, demonstrate the symmetry of true and complementary delays, even when driving 200fF loads. Figure 16.5.5 shows simulated and measured clock-to-output delays as a function of setup and hold time. SAFF shows <100ps sampling window. Hold time is dependent on data slope. It is possible to shorten the hold time by buffering the data, as done in the scan path, shown in Figure 16.5.3.

In comparison to recently-published flip-flops, the modified sense-amplifier flip-flop has the shortest delay, represented by the sum of setup time and clock to output delay, Figure 16.5.6 [7, 8, 9]. Transmission gate master-slave flip-flop (TG M-S) and C²MOS master-slave flip-flop are also used in comparison. The simulations were done using BSIM 3v3 (level 49) CMOS transistor model. Nominal process corner, 25°C and 1.8Vsupply are used. All inputs are driven by large buffers, resulting in 100ps, 20%-80% rise and fall times and outputs are loaded with 200fF. All the flip-flops are optimized for minimum delay with output transistor sizes limited. Power consumption is shown for maximum, average and minimum activities.

Delays, setup and hold times of the flip-flop are measured on the test chip. Simulated and measured data is summarized in Table 16.4.1. To measure flip-flop performance, a simple test structure is implemented on the test chip. The minimum delay between the data arrival and output transition, Figure 16.5.5, is measured indirectly, by changing the clock frequency in the 400-700MHz range and observing the difference of two flip-flop outputs following the inverter chains of different lengths.

References:

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[9] F. Klass, "Semi-Dynamic and Dynamic Flip-Flops with Embedded Logic," Symp. on VLSI Circ, Digest of Technical Papers, pp.108-109, June 1998.

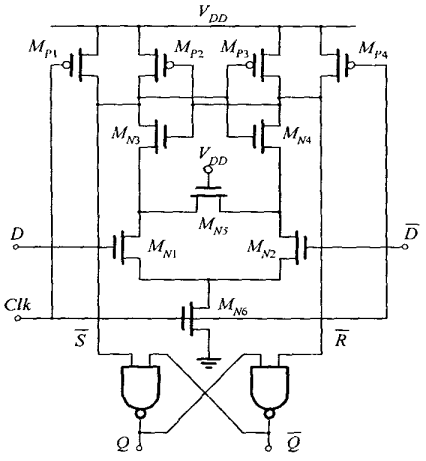

Figure 16.5.1: Sense amplifier-based flip-flop.

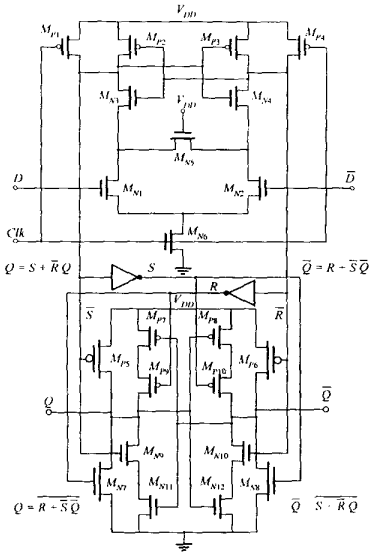

Figure 16.5.2: Modified sense amplifier-based flip-flop.

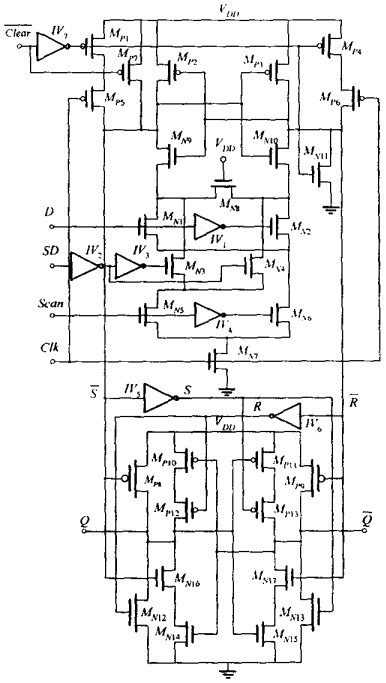

Figure 16.5.3: Sense amplifier-based flip-flop with multiplexed scan and asynch. reset.

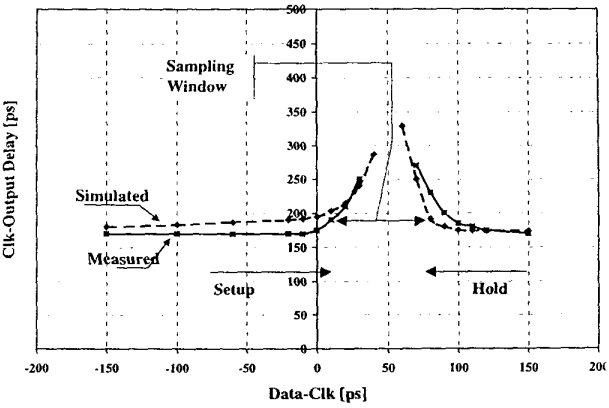

Figure 16.5.5: Measured and simulated clock to-output delay vs setup and hold times.

Figure 16.5.6: See page 468.

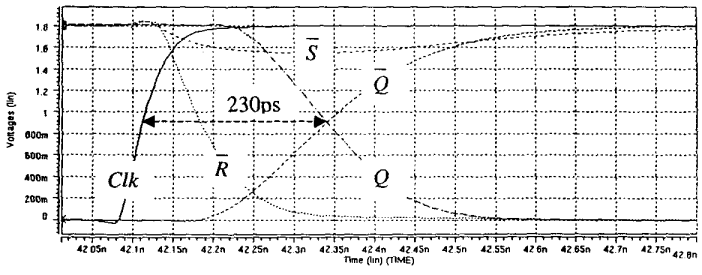

Figure 16.5.4: Typical SAFF waveforms.

Parameter	Simulated, differential C_L = 200fF	Simulated, single-ended load = 2 inverters	Measured, single-ended load = 2 inverters
Rising delay, *Clk-Q*	230ps	165ps	170ps ± 20ps
Falling delay, *Clk-Q*	225ps	175ps	170ps ± 20ps
Setup time	-25ps	0ps	0ps ± 20ps
Hold time	160ps	90ps	80ps ± 20ps
Avg. Power	31µW	29µW	N.A.

Table 16.5.1: Summary of SAFF parameters (Nominal process, postlayout, 1.8V VDD 25°C, 100ps clock and data rise times).

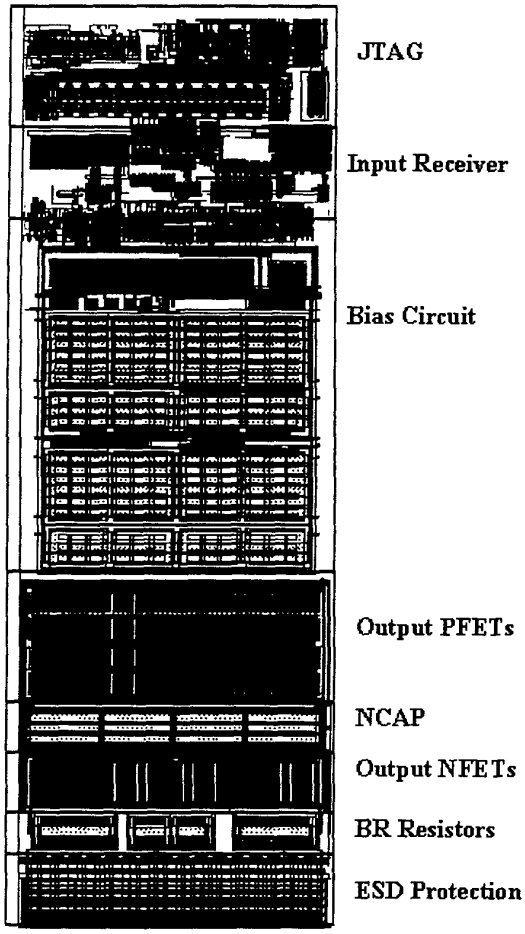

Figure 16.2.7: L2 driver layout.

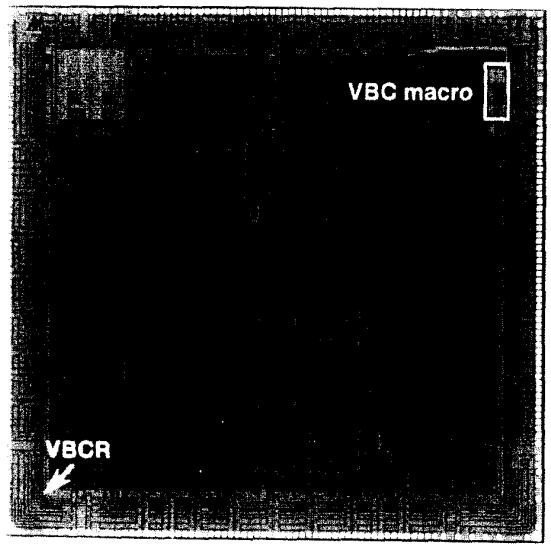

Figure 16.4.4: Chip micrograph.

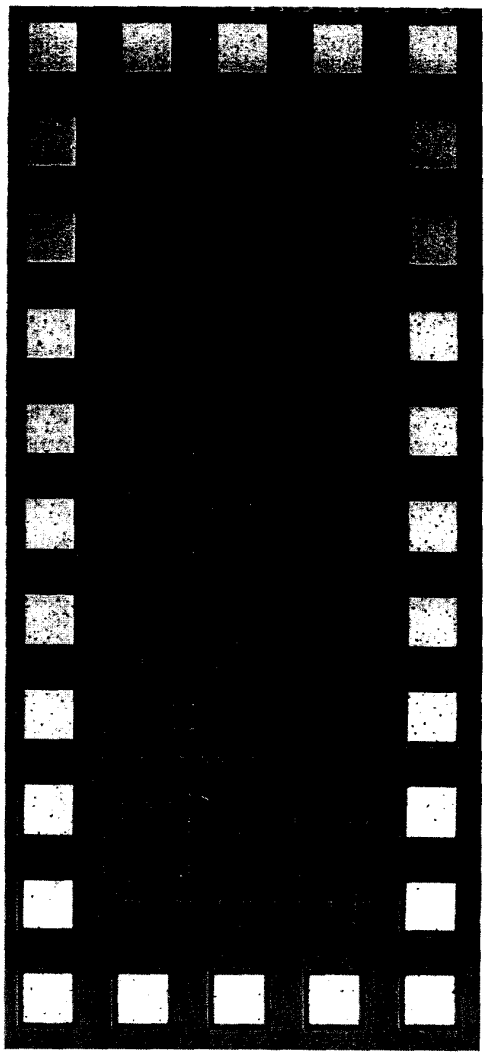

Figure 16.3.7: Chip micrograph.

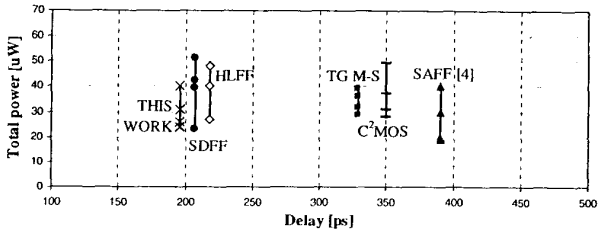

Figure 16.5.6: Comparison of delays and power among different flip-flops.

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