Kenneth Mai

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Education

Ph.D.	Electrical Engineering, Stanford University, expected June 2004 Thesis: "Design and Analysis of Reconfigurable Memories" Advisor: Professor Mark Horowitz
M.S.	Electrical Engineering, Stanford University, 1997
B.S.	Electrical Engineering, with Distinction, Stanford University, 1993

Research Interests

Design and implementation of next-generation computing architectures

High-speed, low-power memory design

CAD tools for memory design, simulation visualization, and verification

Research Experience

1997-present — Research Assistant, Stanford University, Computer Systems Laboratory

Designed architecture, circuits, and layout of a prototype reconfigurable SRAM chip in a 0.18-μm process. The design can emulate various caches, streaming FIFOs, and scratch-pad memories with small performance, area, and power overheads. Designed custom PCB and tested the chip, which ran at 1.1GHz under nominal conditions.

Designed and simulated a reconfigurable, modular computing architecture. The architecture employed coarse-grain reconfigurability in its compute, memory, and interconnect to achieve performance near that of hardwired solutions at a reasonable overhead.

Modeled characteristics of interconnect in future process technologies and projected the effects on computer architecture and CAD tool development.

Designed architecture, circuits, and layout of a prototype low-power SRAM chip. The design used self-timed, post-charge, charge-recycling circuits to achieve sub-1mW power dissipation in a 4KB memory running at 100MHz in a dual-Vt 0.25-μm process.

Designed circuits and layout of various blocks used in research group chips. These chips included low-power interconnect and high-speed I/O designs. Maintained and developed CAD tools for IC design environment.

1997 (summer) — Summer Intern, Texas Instruments
Designed architecture and circuits of a high-speed, multi-port register file

1995 (summer) — Summer Intern, Cypress Semiconductor
Codified design rules for a new generation process technology

Publications

K. Mai, R. Ho, E. Alon, D. Liu, Y. Kim, D. Patil, M. Horowitz, "Architecture and Circuit Techniques for a Reconfigurable Memory Block," To appear in *IEEE Journal of Solid-State Circuits*, November 2004.

H. Lee, C. Yue, S. Palermo, K. Mai, M. Horowitz, "Burst Mode Packet Receiver using a Second Order DLL," To appear in *Digest of Technical Papers, Symposium on VLSI Circuits*, June 2004.

K. Mai, R. Ho, E. Alon, D. Liu, Y. Kim, D. Patil, M. Horowitz, "Architecture and Circuit Techniques for a Reconfigurable Memory Block," *Digest of Technical Papers, IEEE International Solid-State Circuits Conference*, February 2004.

R. Ho, K. Mai, M. Horowitz, "Efficient On-Chip Global Interconnects," *Digest of Technical Papers, Symposium on VLSI Circuits*, June 2003.

R. Ho, K. Mai, M. Horowitz, "Managing Wire Scaling: A Circuit Perspective," *Proceedings of the IEEE International Interconnect Technology Conference*, June 2003.

R. Ho, K. Mai, M. Horowitz, "The Future of Wires," *Proceedings of the IEEE*, Vol. 89, Issue 4, April 2001.

K. Mai, T. Paaske, N. Jayasena, R. Ho, W. Dally, M. Horowitz, "Smart Memories: A Modular Reconfigurable Architecture," *Proceedings of the 27th International Symposium on Computer Architecture*, June 2000.

R. Ho, K. Mai, H. Kapadia, M. Horowitz, "Interconnect Scaling Implications for CAD," *Digest of Technical Papers, IEEE/ACM International Conference on Computer-Aided Design*, November 1999.

K. Mai, T. Mori, B. Amrutur, R. Ho, B. Wilburn, M. Horowitz, I. Fukushi, T. Izawa, S. Mitarai, "Low-Power SRAM Design Using Half-Swing Pulse-Mode Techniques," *IEEE Journal of Solid-State Circuits*, Vol. 33, Issue 11, November 1998.

R. Ho, B. Amrutur, K. Mai, B. Wilburn, T. Mori, M. Horowitz, "Applications of On-Chip Samplers for Test and Measurement of Integrated Circuits," *Digest of Technical Papers, Symposium on VLSI Circuits*, June 1998.

T. Mori, B. Amrutur, K. Mai, M. Horowitz, I. Fukushi, T. Izawa, S. Mitarai, "A 1V 0.9mW at 100MHz 2k*16b SRAM Utilizing a Half-Swing Pulsed Decoder and Write-Bus Architecture in 0.25-μm Dual-Vt CMOS," *Digest of Technical Papers, IEEE International Solid State Circuits Conference*, February 1998.

Teaching Experience

2002-2003	Teaching Fellow, Stanford University, EE 272A, "VLSI Design Projects"
1995-1996	Teaching Assistant, Stanford University, EE 272A/B, "VLSI Design Projects"
1994-1996	Teaching Assistant, Stanford University, EE 271, "Introduction to VLSI Design"
1994	Teaching Assistant, Stanford University, EE 275, "Logic Design"
1994 (summer)	Teaching Fellow, Stanford University, EE 275, "Logic Design"

Honors

2000-2004	Philips FMA program sponsored student
1995-1996	Stanford Centennial Teaching Assistant Award for Outstanding Teaching
1993	Member of Phi Beta Kappa
1992	Member of Tau Beta Pi

References

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