A Tracking PLL with an FIR Loop Filter

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To stabilize the feedback loop of a PLL a lead-lag filter is used, implemented by driving the charge-pump current to a series resistor capacitor network [1]. While many designs have created the needed resistor using the resistance of an amplifier [2], and even made this resistor track the operating frequency [3], all these loops suffer from periodic noise on the control voltage caused by the small ripple current inevitable in most charge-pump designs. One alternative to using a resistor is to use a finite-impulse-response (FIR) filter to generate the needed zero. In this design, the charge-pump current is added to the integrating capacitor and then a fraction A (close to 1) is subtracted from the capacitor at a later time. The net effect is that 1-A of the charge-pump current is integrated on the capacitor, and the rest is not integrated; it acts as the linear term to stabilize the loop.

The delayed charge-pump current can be generated by many methods as shown in Figure 1: (a) using two delay lines to delay the clock inputs to an additional phase-frequency detector (PFD), (b) delaying the up and down pulses from the existing PFD, and (c) delaying the charge from the second charge pump. An implementation of (c), independently conceived, is presented by Lee and Razavi [5] for wireless application. This paper explores using FIR filters for link and processor applications that use ring oscillators with small multiplication factors. In particular, we extend our previous work on adaptive-supply VCO [4] to use a FIR filter by using the topology in Figure 1a.

Referring to Figure 1, the closed-loop transfer function (including loop delay T_D) is

$$H(s) = \frac{(1 - Ae^{-Ts})e^{-T_D s}}{(2\pi CNs^2)/(I_0 K) + (1 - Ae^{-Ts})e^{-T_D s}} \quad (1),$$

where K is the voltage controlled oscillator (VCO) gain, I_0 is the charge-pump current, A is the filter coefficient for the second tap, T is the delay between the first and second tap in the FIR-filter, T_D is the propagation delay of the feedback clock, C is the capacitance of the control-voltage node, and N is the multiplication factor of the loop. One can use a root-locus plot to guide design decisions as shown in Figure 2. The most interesting design points are when the dominant poles (that start at the origin) are on the circle around the zero, $s = \ln(A)/T$, generated by the filter. A design with the roots on that circle, $T=1/f_{VCO}$ and A=0.8, will always be stable and will have a maximum system bandwidth of $f_{VCO}/10$.

Observations of eq. (1) suggest that the loop dynamics can track the operating frequency with some additions to the design. First, by letting the VCO control voltage also control the delay of the two delay-lines, the delay T will track the reference clock period. Hence, the product, Ts, will be constant for a frequency with a given ratio to the operating frequency in eq.(1). Next, the expression $(2\pi CNs^2)/(I_0 K)$ needs to be constant. We achieve this by letting the charge-pump currents track the square of the VCO frequency. Maintaining the $T_D s$ product constant across the operating frequency range is harder. One approach to circumvent this difficulty is to assume a small loop delay, since it is not easy to let the operating frequency control this delay without unwanted side effects.

It is interesting to note that one can set up a stable loop for N=1 to 4 without scaling the delay of the delay-lines or other loop parameters. If we assume that for N=1 the pole pair is a double-pole at the left side of the circle around the zero in Figure 2 and normalize their position to the position of the zero, then the poles are at approximately $s_{NORM} = -2 + j0$, and the system has a normalized ω_n=2 and ζ=1. When changing N to 2, the pole pair moves to approximately $s_{NORM} = -1 \pm j$, where ω_n and ζ decrease to 1.41 and 0.707, respectively. Finally, the pole pair moves to $s_{NORM} = -0.2 \pm j0.7$, for N=4, and the ω_n drops to 0.737 and ζ to 0.383.

While this wide stability and independence of technology parameters is appealing, the downside of using an FIR filter is that some errors are amplified by the 1/(1-A) gain of the loop. One error is that the difference in phase offsets between the two phase detector / charge pump combinations is amplified. When the input phase offsets of the taps do not match, the closed loop will have a phase offset of 1/(1-A)*(tap0_phase_offset - A*tap1_phase_offset). Thus this loop probably cannot be used directly where precise phase alignment is needed.

This difference in phase offsets also means that when the loop is in lock, the charge pumps will 'fight' each other to reach a stable state. In other words, the two charge-pumps will be injecting some small current into the loop each update cycle. If the delay matches the reference clock period, then the 'new' charge quanta from the first charge-pump and the 'old' charge quanta from the second charge-pump will cancel each other and there will, to first order, be no ripple. Some ripple will result from the very slight difference in shape in the current waveforms. However, if the delay between the charge-pumps is not equal to the reference clock periods, the two taps will add currents at different times, causing ripple/harmonics on the control voltage at frequencies that are multiples of the PFD operation frequency, $f=n*f_{PFD}$; therefore, if the delay does not scale with N, the loop will be stable, but the clocks produced are likely to have large frequency spurs. Measured results indicate that this is indeed the case. At f_{VCO}=400MHz, N=4, four consecutive clock periods were measured to be 2.545ns, 2.540ns, 2.500ns, and 2.415ns.

Figure 3 illustrates the prototype PLL built in the National 0.25-μm process. This PLL uses a simple FIR filter where the delay is one VCO clock cycle, A = 0.8, and takes advantage of regulated-supply techniques [4] to simplify the design. Using a regulated-supply to control the five-stage VCO and the two ten-stage VCDLs guarantees that the delay of the second tap will match the VCO period across all operating frequencies, for N=1. Using the control voltage to bias the charge-pump as is done in [4], scales I_0 with the square of the VCO frequency. Measured loop performance shows that for a given N, ζ stays relatively constant and ω_n tracks with the frequencies. Furthermore, across the different multiplication factors, the scaling of ζ and ω_n essentially follows what the theory predicts.

The PLL occupies 0.065 mm^2 of area and dissipates 22.8 mW of power at 2.5V. Figure 4 shows the die photo. The loop operates from 75 MHz to 870 MHz. Figure 5 shows the loop jitter (34 ps pk-pk) while operating at 700 MHz with a quiet supply. These numbers are worse than those obtained in [4], an adaptive supply design that used the amplifier's output resistance to compensate the loop. The extra delay lines in the FIR filter cause the power and area to be larger, and the possible noise gain means that some of the transistors need to be scaled up in size. Thus, this architecture should be used only if low control ripple is essential.

References

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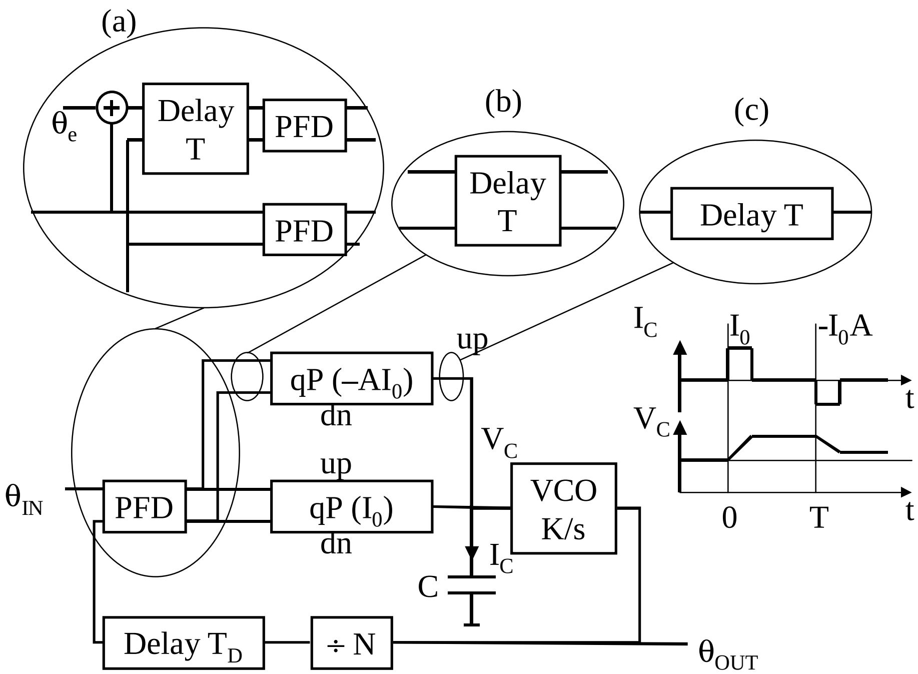

Figure 1 PLL with FIR Loop-Filter

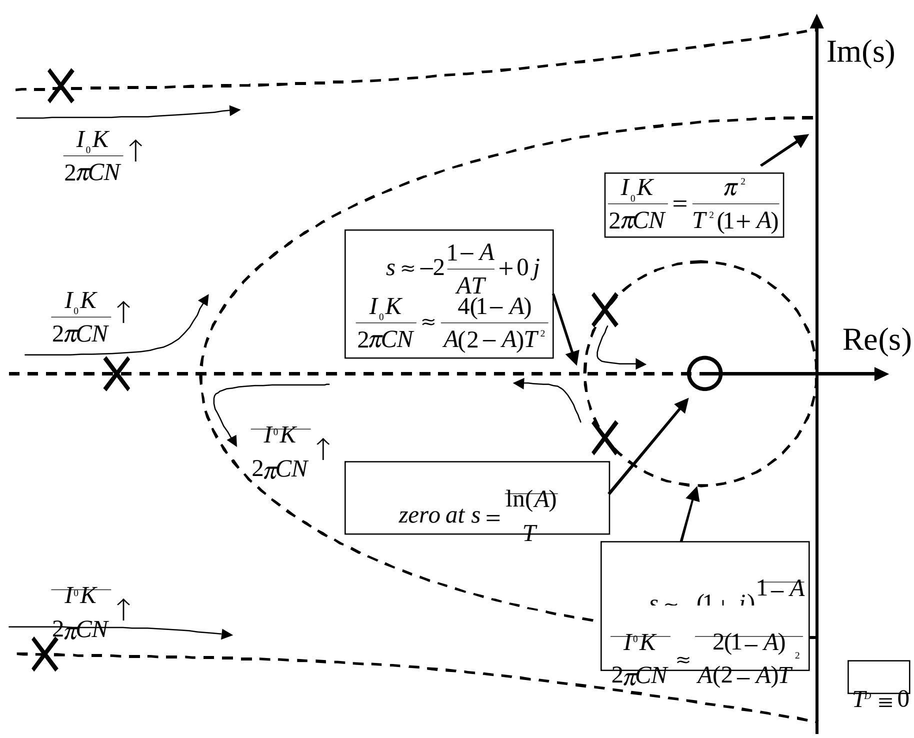

Figure 2 Schematic Root-Locus

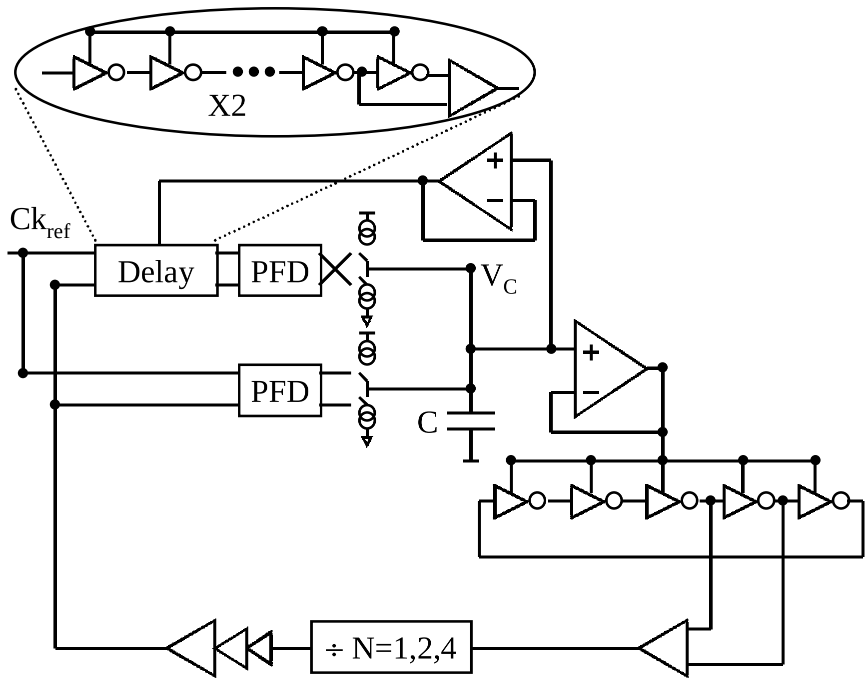

Figure 3 PLL Block Diagram

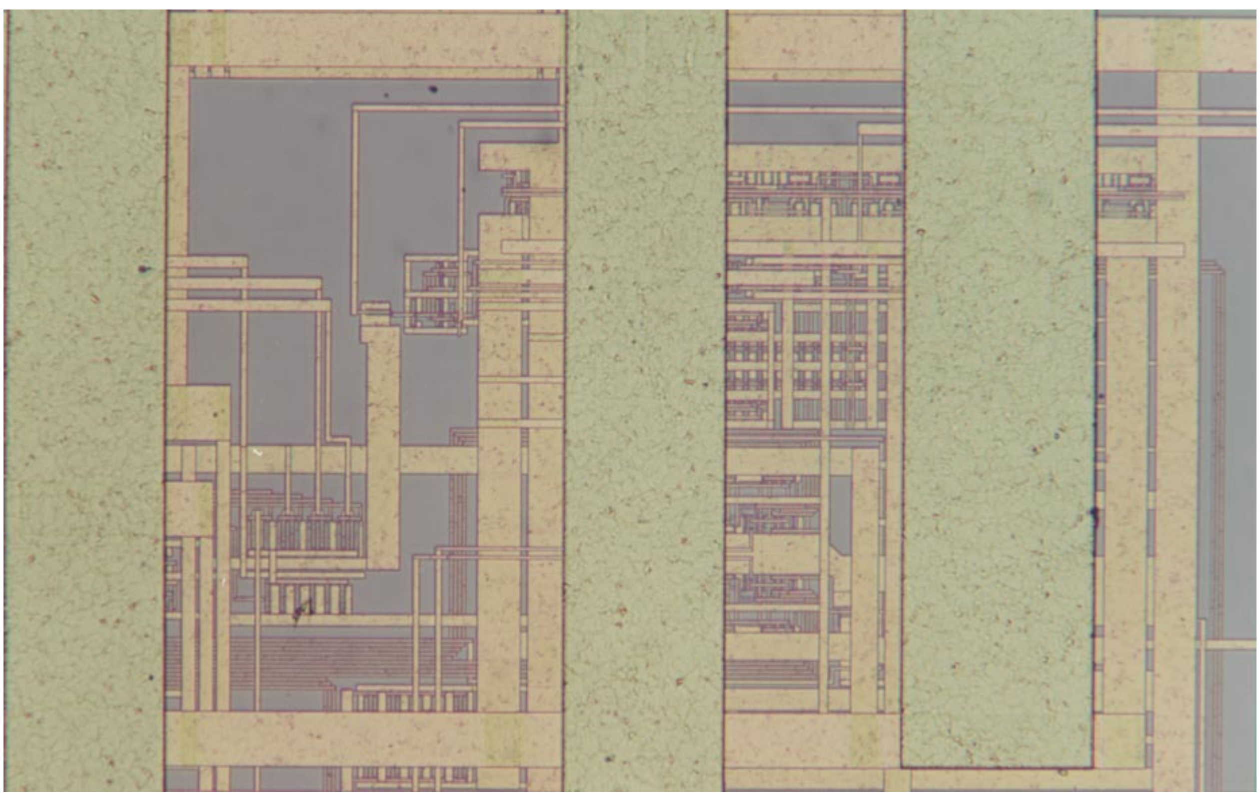

Figure 4 Chip Micrograph

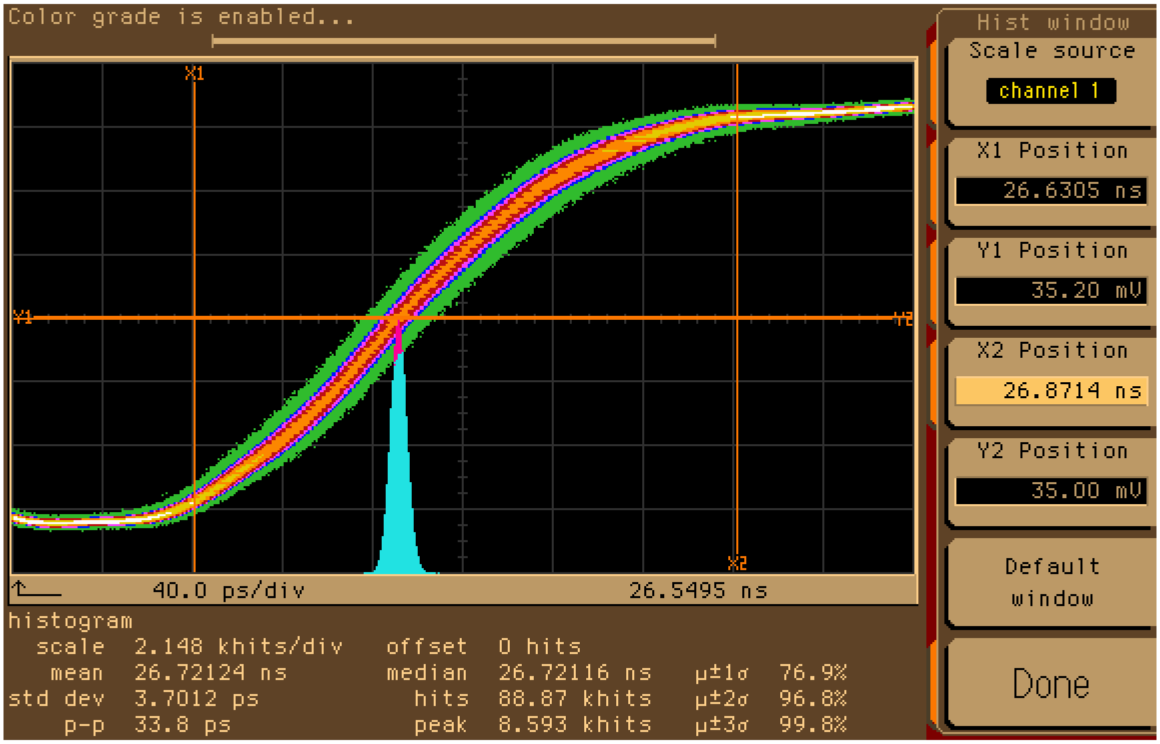

Figure 5 Jitter Histogram